Amendments to the Specification:

Please amend the paragraph beginning at page 51, lines 18-24, as follows:

Fig. 32 is a view schematically showing a layout of an embedded device to which the ferroelectric memory device of the above embodiment is applied. In this example, an embedded device 2000 includes a flash memory 90, a processor 94, and an analog circuit 96 which are formed on SOG (Sea of ~~Gates)~~Gates) 92. An SRAM may be included in combination.